WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor host material, having a valence-band energy, E_V, a conduction-band energy, E_C, and an energy gap, E_G;

a deep-level region, formed in said host material, the deep-level region having one or more deep-level state(s) with energy at least $0.05E_G$ above E_V and at least $0.05E_G$ below E_C; and,

means for injecting carriers into the deep-level region to produce transition(s) between one or more of the deep-level state(s) and the conduction- or valence-band or another deep-level of the host material.

2. A semiconductor device, as defined in claim 1, wherein the deep-level region comprises an optically-active region in which transitions between deep-level state(s) and the conduction- or valence-band or another deep-level of the host material produce or absorb photons.

3. A semiconductor device, as defined in claim 1, wherein the means for injecting carriers into the deep-level region directly injects carriers into one or more of the deep-level state(s)

without having to first enter the deep-level region's conduction or valence band.

4. A semiconductor device, as defined in claim 1, wherein the host material is an elemental semiconductor.

5. A semiconductor device, as defined in claim 1, wherein the host material comprises a direct bandgap elemental semiconductor material.

6. A semiconductor device, as defined in claim 1, wherein the host material comprises an indirect bandgap elemental semiconductor material.

7. A semiconductor device, as defined in claim 1, wherein the host material is a compound semiconductor.

8. A semiconductor device, as defined in claim 1, wherein the host material comprises a direct bandgap compound semiconductor material.

9. A semiconductor device, as defined in claim 1, wherein the host material comprises an indirect bandgap compound semiconductor material.

10. A semiconductor device, as defined in claim 1, wherein the host material is an elemental semiconductor from Group IVA of the periodic table.

11. A semiconductor device, as defined in claim 1, wherein the host material is one of: C, Si, Ge, Sn, or Pb.

12. A semiconductor device, as defined in claim 1, wherein the host material comprises a direct bandgap alkali-halide compound.

13. A semiconductor device, as defined in claim 1, wherein the host material comprises an indirect bandgap alkali-halide compound.

14. A semiconductor device, as defined in claim 1, wherein the host material is an alkali-halide compound.

15. A semiconductor device, as defined in claim 1, wherein the host material is one of: LiF, LiCl, LiBr, LiI, LiAt, NaF, NaCl, NaBr, NaI, NaAt, KF, KCl, KBr, KI, or KAt.

16. A semiconductor device, as defined in claim 1, wherein the host material comprises a direct bandgap binary semiconductor compound.

17. A semiconductor device, as defined in claim 1, wherein the host material comprises an indirect bandgap binary semiconductor compound.

18. A semiconductor device, as defined in claim 1, wherein the host material is a binary compound formed from Groups IIB and VIA of the periodic table.

19. A semiconductor device, as defined in claim 1, wherein the host material is one of: ZnO, ZnS, ZnSe, ZnTe, ZnPo, CdO, CdS, CdSe, CdTe, CdPo, HgO, HgS, HgSe, HgTe, or HgPo.

20. A semiconductor device, as defined in claim 1, wherein the host material is a binary compound formed from Groups IIIA and VA of the periodic table.

21. A semiconductor device, as defined in claim 1, wherein the host material is one of: BN, BP, BAs, BSb, BBi, AlN, AlP, AlAs, AlSb, AlBi, GaN, GaP, GaAs, GaSb, GaBi, InN, InP, InAs, InSb, InBi, TlN, TlP, TlAs, TlSb, or TlBi.

22. A semiconductor device, as defined in claim 1, wherein the host material is a binary compound formed from Group IVA of the periodic table.

23. A semiconductor device, as defined in claim 1, wherein the host material is one of: SiC or SiGe.

24. A semiconductor device, as defined in claim 1, wherein the host material is a binary compound formed from Groups IVA and VIA of the periodic table.

25. A semiconductor device, as defined in claim 1, wherein the host material is one of: PbO, PbS, PbSe, PbTe, PbPo, SnO, SnS, SnSe, SnTe, or SnPo.

26. A semiconductor device, as defined in claim 1, wherein the host material comprises a direct bandgap ternary semiconductor compound.

27. A semiconductor device, as defined in claim 1, wherein the host material comprises an indirect bandgap ternary semiconductor compound.

28. A semiconductor device, as defined in claim 1, wherein the host material is a ternary compound formed from Groups IIB, IIB, and VIA of the periodic table.

29. A semiconductor device, as defined in claim 1, wherein the host material is one of: ZnCdO, ZnCdS, ZnCdSe, ZnCdTe, ZnCdPo, ZnHgO, ZnHgS, ZnHgSe, ZnHgTe, ZnPo, CdHgO, CdHgS, CdHgSe, CdHgTe, or CdHgPo.

30. A semiconductor device, as defined in claim 1, wherein the host material is a ternary compound formed from Groups IIB, VIA, and VIA of the periodic table.

31. A semiconductor device, as defined in claim 1, wherein the host material is one of: ZnOS, ZnOSe, ZnOTe, ZnSSe, ZnSTe, ZnSeTe, CdOS, CdOSe, CdOTe, CdSSe, CdSTe, CdSeTe, HgOS, HgOSe, HgOTe, HgSSe, HgSTe, or HgSeTe.

32. A semiconductor device, as defined in claim 1, wherein the host material is a ternary compound formed from Groups IIIA, IIIA, and VA of the periodic table.

33. A semiconductor device, as defined in claim 1, wherein the host material is one of: InGaAs, InGaP, InGaN, InGaSb, AlGaAs, AlGaP, AlGaN, AlGaSb, InAlAs, InAlP, InAlN, or InAlSb.

34. A semiconductor device, as defined in claim 1, wherein the host material is a ternary compound formed from Groups IIIA, VA, and VA of the periodic table.

35. A semiconductor device, as defined in claim 1, wherein the host material is one of: InAsP, InAsN, InAsSb, InPN, InPSb, InNSb, GaAsP, GaAsN, GaAsSb, GaPN, GaPSb, GaNSb, AlAsP, AlAsN, AlAsSb, AlPN, AlPSb, or AlNSb.

36. A semiconductor device, as defined in claim 1, wherein the host material is a ternary compound formed from Groups IVA, IVA, and VIA of the periodic table.

37. A semiconductor device, as defined in claim 1, wherein the host material is one of: SnPbS, SnPbSe, or SnPbTe.

38. A semiconductor device, as defined in claim 1, wherein the host material is a ternary compound formed from Groups IVA, VIA, and VIA of the periodic table.

39. A semiconductor device, as defined in claim 1, wherein the host material is one of: SnSSe, SnSTe, SnSeTe, PbSSe, PbSTe, or PbSeTe.

40. A semiconductor device, as defined in claim 1, wherein the host material comprises a direct bandgap quaternary semiconductor compound.

41. A semiconductor device, as defined in claim 1, wherein the host material comprises an indirect bandgap quaternary semiconductor compound.

42. A semiconductor device, as defined in claim 1, wherein the host material includes three group IIB constituents and one group VIA constituent from the periodic table.

43. A semiconductor device, as defined in claim 1, wherein the host material includes two group IIB constituents and two group VIA constituents from the periodic table.

44. A semiconductor device, as defined in claim 1, wherein the host material includes one group IIB constituent and three group VIA constituents from the periodic table.

45. A semiconductor device, as defined in claim 1, wherein the host material includes three group IIIA constituents and one group VA constituent from the periodic table.

46. A semiconductor device, as defined in claim 1, wherein the host material includes two group IIIA constituents and two group VA constituents from the periodic table.

47. A semiconductor device, as defined in claim 1, wherein the host material includes one group IIIA constituent and three group VA constituents from the periodic table.

48. A semiconductor device, as defined in claim 1, wherein the host material is one of InGaAlAs, InGaAlP, InGaAlN, or InGaAlSb.

49. A semiconductor device, as defined in claim 1, wherein the host material is one of InGaAsP, InGaAsN, InGaAsSb, InGaPN, InGaPSb, InGaNSb, AlGaAsP, AlGaAsN, AlGaAsSb, AlGaPN, AlGaPSb, AlGaNSb, InAlAsP, InAlAsN, InAlAsSb, InAlPN, InAlPSb, or InAlNSb.

50. A semiconductor device, as defined in claim 1, wherein the host material is one of InAsPN, InAsPSb, InAsNSb, InPNSb,

GaAsPN, GaAsPSb, GaAsNSb, GaPNSb, AlAsPN, AlAsPSb, AlAsNSb, or AlPNSb.

51. A semiconductor device, as defined in claim 1, wherein the host material includes three group IVA constituents and one group VIA constituent.

52. A semiconductor device, as defined in claim 1, wherein the host material includes two group IVA constituents and two group VIA constituents.

53. A semiconductor device, as defined in claim 1, wherein the host material includes one group IVA constituent and three group VIA constituents.

54. A semiconductor device, as defined in claim 1, wherein the host material comprises an alkali-halide material comprised of any number of constituents from groups I and VII.

55. A semiconductor device, as defined in claim 1, wherein the host material comprises a compound semiconductor material comprised of any number of constituents from groups IIB and VIA.

56. A semiconductor device, as defined in claim 1, wherein the host material comprises a compound semiconductor material comprised of any number of constituents from groups IIIA and VA.

57. A semiconductor device, as defined in claim 1, wherein the host material comprises a compound semiconductor material comprised of any number of constituents from group IVA.

58. A semiconductor device, as defined in claim 1, wherein the host material comprises a compound semiconductor material comprised of any number of constituents from groups IVA and VIA.

59. A semiconductor device, as defined in claim 1, wherein the host material comprises GaAs.

60. A semiconductor device, as defined in claim 1, wherein the host material comprises InP.

61. A semiconductor device, as defined in claim 1, wherein the host material comprises InGaAs.

62. A semiconductor device, as defined in claim 1, wherein the host material comprises InGaP.

63. A semiconductor device, as defined in claim 1, wherein the host material comprises InGaAlAs.

64. A semiconductor device, as defined in claim 1, wherein the host material comprises InGaAsP.

65. A semiconductor device, as defined in claim 1, wherein the host material comprises Si.

66. A semiconductor device, as defined in claim 1, wherein the host material comprises GaP.

67. A semiconductor device, as defined in claim 1, wherein the host material comprises SiGe.

68. A semiconductor device, as defined in claim 1, wherein the host material comprises AlGaAs.

69. A semiconductor device, as defined in claim 1, wherein the host material comprises AlGaAsP.

70. A semiconductor device, as defined in claim 1, wherein the host material comprises SiC.

71. A semiconductor device, as defined in claim 1, wherein the host material comprises GaN.

72. A semiconductor device, as defined in claim 1, wherein the host material comprises InN.

73. A semiconductor device, as defined in claim 1, wherein the host material comprises GaAsN.

74. A semiconductor device, as defined in claim 1, wherein the host material comprises InGaN.

75. A semiconductor device, as defined in claim 1, wherein the host material comprises GaAlN.

76. A semiconductor device, as defined in claim 1, wherein the host material comprises InGaAlN.

77. A semiconductor device, as defined in claim 1, wherein the host material comprises InGaAsN.

78. A semiconductor device, as defined in claim 1, wherein the host material comprises GaAlAsN.

79. A semiconductor device, as defined in claim 1, wherein the host material comprises InGaAlAsN.

80. A semiconductor device, as defined in claim 1, wherein the injected carriers produce deep-level-to-valence-band transitions.

81. A semiconductor device, as defined in claim 80, wherein the means for injecting carriers injects carriers into both the deep-level state(s) and the valence band.

82. A semiconductor device, as defined in claim 1, wherein the injected carriers produce conduction-band-to-deep-level transitions.

83. A semiconductor device, as defined in claim 82, wherein the means for injecting carriers injects carriers into both the deep-level state(s) and the conduction band.

84. A semiconductor device, as defined in claim 1, wherein the injected carriers produce deep-level-to-deep-level transitions.

85. A semiconductor device, as defined in claim 84, wherein the means for injecting carriers injects carriers into both deep-level (upper and lower) state(s) in a deep-level-to-deep-level transition.

86. A semiconductor device, as defined in claim 1, wherein the means for injecting carriers comprises an n-type region.

87. A semiconductor device, as defined in claim 1, wherein the means for injecting carriers comprises a p-type region.

88. A semiconductor device, as defined in claim 1, wherein the means for injecting carriers comprises a metallic region.

89. A semiconductor device, as defined in claim 1, wherein the means for injecting carriers comprises an oxide region.

90. A semiconductor device, as defined in claim 1, wherein the means for injecting carriers comprises a Schottky contact.

91. A semiconductor device, as defined in claim 1, wherein the means for injecting carriers comprises a region of semiconductor material different from the host material.

92. A semiconductor device, as defined in claims 86-91, wherein the Fermi-level, under equilibrium or under nonequilibrium operating conditions, of the means for injecting carriers lies within the bandgap of the material that comprises the deep-level-region.

93. A semiconductor device, as defined in claims 86-91, wherein the Fermi-level, under equilibrium or under nonequilibrium operating conditions, of the means for injecting carriers lies within $0.75E_G$ of the deep-level state(s) in the deep-level-region that participate in transitions with the valence or conduction bands.

94. A semiconductor device, as defined in claims 86-91, wherein the Fermi-level, under equilibrium or under nonequilibrium operating conditions, of the means for injecting carriers lies within $0.5E_G$ of the deep-level state(s) in the deep-level-region that participate in transitions with the valence or conduction bands.

95. A semiconductor device, as defined in claims 86-91, wherein the Fermi-level, under equilibrium or under nonequilibrium operating conditions, of the means for injecting carriers lies within $0.25E_G$ of the deep-level state(s) in the deep-level-region that participate in transitions with the valence or conduction bands.

96. A semiconductor device, as defined in claim 1, wherein the deep-level state(s) in the deep-level region are created, at least in part, by substitutional impurities.

97. A semiconductor device, as defined in claim 96, wherein the deep-level state(s) in the deep-level region are created, at least in part, by Cr substitution at anion or cation sites in the host material.

98. A semiconductor device, as defined in claim 96, wherein the deep-level state(s) in the deep-level region are created, at least in part, by Fe substitution at anion or cation sites in the host material.

99. A semiconductor device, as defined in claim 96, wherein the deep-level state(s) in the deep-level region are created, at least in part, by O substitution at anion or cation sites in the host material.

100. A semiconductor device, as defined in claim 96, wherein the deep-level state(s) in the deep-level region are created, at

least in part, by Cu substitution at anion or cation sites in the host material.

101. A semiconductor device, as defined in claim 1, wherein the deep-level state(s) in the deep-level region are created, at least in part, by low-temperature growth of the host material.

102. A semiconductor device, as defined in claim 1, wherein the deep-level state(s) in the deep-level region are created, at least in part, by nonstoichiometric (anion-rich or cation-rich) conditions within the deep-level region.

103. A semiconductor device, as defined in claim 1, wherein the deep-level state(s) in the deep-level region are created, at least in part, by antisites in the host material.

104. A semiconductor device, as defined in claim 100, wherein the deep-level state(s) in the deep-level region are created, at least in part, by cation-on-anion sites in the host material.

105. A semiconductor device, as defined in claim 101, wherein the deep-level state(s) in the deep-level region are created, at least in part, by substitution of group V species on group III sites of a III-V host material.

106. A semiconductor device, as defined in claim 100, wherein the deep-level state(s) in the deep-level region are created, at least in part, by substitution of As on group III sites of a III-arsenide host material.

107. A semiconductor device, as defined in claim 100, wherein the deep-level state(s) in the deep-level region are created, at least in part, by substitution of P on group III sites of a III-phosphide host material.

108. A semiconductor device, as defined in claim 100, wherein the deep-level state(s) in the deep-level region are created, at least in part, by substitution of N on group III sites of a III-nitride host material.

109. A semiconductor device, as defined in claim 100, wherein the deep-level state(s) in the deep-level region are created, at least in part, by anion-on-cation sites in the host material.

110. A semiconductor device, as defined in claim 1, wherein the deep-level state(s) in the deep-level region are created, at least in part, by vacancies in the host material.

111. A semiconductor device, as defined in claim 110, wherein the deep-level state(s) in the deep-level region are created, at least in part, by cation vacancies in the host material.

112. A semiconductor device, as defined in claim 110, wherein the deep-level state(s) in the deep-level region are created, at least in part, by anion vacancies in the host material.

113. A semiconductor device, as defined in claim 1, wherein the deep-level state(s) in the deep-level region are created, at least in part, by interstitial species in the host material.

114. A semiconductor device, as defined in claim 1, wherein the deep-level state(s) in the deep-level region are created, at least in part, by dislocations in the host material.

115. A semiconductor device, as defined in claim 1, wherein the deep-level state(s) in the deep-level region are created, at least in part, by complexes of two-or-more of (i) substitutional impurities, (ii) antisites, (iii) vacancies, (iv) interstitials, and/or (v) dislocations in the host material.

116. A semiconductor device, as defined in claim 1, wherein the host material is GaAs, and the deep-level transition(s) produce wavelength(s) longer than 0.85 μm.

117. A semiconductor device, as defined in claim 1, wherein the host material is GaAs, and the deep-level transition(s) produce wavelength(s) in the range of 1.2 - 1.7 μm.

118. A semiconductor device, as defined in claim 117, integrated with a plurality of GaAs MESFETs, all realized on a single GaAs substrate.

119. A semiconductor device, as defined in claim 117, integrated with a plurality of GaAs electronic circuits, all realized on a single GaAs substrate.

120. A semiconductor device, as defined in claim 117, integrated with a plurality of Si semiconductor devices using growth of GaAs on Si.

121. A semiconductor device, as defined in claim 117, integrated with a plurality of Si semiconductor devices using growth of GaAs on Si, with intermediate layer or layers between the GaAs and Si.

122. A semiconductor device, as defined in claim 1, wherein the host material is GaP, and the deep-level transitions produce wavelengths in the range 1.2 - 1.7 μm.

123. A semiconductor device, as defined in claim 1, wherein the host material is GaP, and the deep-level transitions produce wavelengths in the visible range (0.2-0.8μm).

124. A semiconductor device, as defined in claim 123, wherein the GaP host material is grown on a lattice-matched Si substrate.

125. A semiconductor device, as defined in claim 123, wherein the GaP host material is grown on a Si substrate with an intermediate layer or layers between the GaP and the Si.

126. A semiconductor device, as defined in claims 124-125, wherein the Si substrate supports a plurality of monolithically-fabricated Si semiconductor devices.

127. A method for making an optically-active semiconductor device, comprising:

providing a semiconductor host material, having a valence-band energy, E_V, a conduction-band energy, E_C, and an energy gap, $E_G = E_C - E_V$;

processing a region of said host material to create an optically-active region wherein a conduction-band-to-deep-level or deep-level-to-valence-band or deep-level-to-deep-level transition produces light of a desired wavelength; and,

abutting the optically-active region with a material selected to enhance carrier transport that supports the desired light-producing transition.

128. A method for making a deep-level-semiconductor-device, comprising:

providing a semiconductor host material, having a valence-band energy, E_V, a conduction-band energy, E_C, and an energy gap, $E_G = E_C - E_V$;

processing to create a deep-level region containing deep-level energy state(s) useful for electrical or optoelectronic or optical devices; and,

abutting the deep-level region with a material selected to enhance carrier transport that supports desired transition(s) involving one or more of the deep-level state(s).

129. A method for making a deep-level-semiconductor-device, as defined in claims 127-128, wherein the host material is grown on a second semiconductor material.

130. A method for making a deep-level-semiconductor-device, as defined in claim 129, wherein the second semiconductor material is Si.

131. A method for making a deep-level-semiconductor-device, as defined in claim 130, further comprising forming a plurality of monolithic devices in said second semiconductor material.

132. A method for making a semiconductor device, as defined in claims 127-128, wherein providing a host material comprises growing a binary compound semiconductor material.

133. A method for making a semiconductor device, as defined in claim 132, wherein the compound semiconductor material comprises GaAs.

134. A method for making a semiconductor device, as defined in claim 133, wherein the GaAs is grown on a Si substrate, with an optional intermediate layer.

135. A method for making a semiconductor device, as defined in claim 132, wherein the compound semiconductor material comprises GaP.

136. A method for making a semiconductor device, as defined in claim 135, wherein the GaP is grown on a Si substrate, with an optional intermediate layer.

137. A method for making a semiconductor device, as defined in claims 127-128, wherein providing a host material comprises growing a ternary compound semiconductor material.

138. A method for making a semiconductor device, as defined in claims 127-128, wherein providing a host material comprises growing a quaternary compound semiconductor material.

139. A method for making a semiconductor device, as defined in claims 127-128, wherein processing a region of said host material to create a deep-level region comprises growing the deep-level region under low-temperature growth conditions.

140. A method for making a semiconductor device, as defined in claims 127-128, wherein processing a region of said host material to create a deep-level region comprises growing the deep-level region under nonstoichiometric (anion-rich or cation-rich) growth conditions.

141. A method for making a semiconductor device, as defined in claims 127-128, wherein processing a region of said host material to create a deep-level region comprises introducing substitutional impurities while growing the deep-level region.

142. A method for making a semiconductor device, as defined in claims 127-128, wherein processing a region of said host material to create a deep-level region comprises adjusting growth conditions to introduce antisites while growing the deep-level region.

143. A method for making a semiconductor device, as defined in claims 127-128, wherein processing a region of said host material to create a deep-level region comprises adjusting

growth conditions to introduce vacancies while growing the deep-level region.

144. A method for making a semiconductor device, as defined in claims 127-128, wherein processing a region of said host material to create a deep-level region comprises adjusting growth conditions to introduce dislocations while growing the deep-level region.

145. A method for making a semiconductor device, as defined in claims 127-128, wherein processing a region of said host material to create a deep-level region comprises introducing species (anions, cations, or impurities) on interstitial sites while growing the deep-level region.

146. A method for making a semiconductor device, as defined in claims 127-128, wherein processing a region of said host material to create a deep-level region comprises introducing two or more of (i) substitutional impurities, (ii) antisites, (iii) vacancies, (iv) interstitials, and/or (v) dislocations into the deep-level region.

147. A method for making a semiconductor device, as defined in claims 127-128, wherein processing a region of said host material to create a deep-level region includes one or more heat treatments.

148. A method for making a semiconductor device, as defined in claims 127-128, wherein abutting the deep-level region with a

material selected to enhance carrier transport comprises abutting the deep-level region with a material that enhances carrier transport into both upper and lower states of the desired transition(s).

149. A method for making a semiconductor device, as defined in claims 127-128, wherein abutting the deep-level region with a material selected to enhance carrier transport comprises abutting one portion of the deep-level region with a material that enhances carrier transport into an upper state of the desired transition(s) and abutting another side of the deep-level region with a material that enhances carrier transport into a lower state of the desired transition(s).

150. A method for making a semiconductor device, as defined in claims 127-128, wherein abutting the deep-level region with a material selected to enhance carrier transport comprises abutting a portion of the deep-level region with an n-type material.

151. A method for making a semiconductor device, as defined in claims 127-128, wherein abutting the deep-level region with a material selected to enhance carrier transport comprises abutting a portion of the deep-level region with a p-type material.

152. A method for making a semiconductor device, as defined in claims 127-128, wherein abutting the deep-level region with a

material selected to enhance carrier transport comprises abutting a portion of the deep-level region with a metal.

153. A method for making a semiconductor device, as defined in claims 127-128, wherein abutting the deep-level region with a material selected to enhance carrier transport comprises abutting a portion of the deep-level region with an oxide material.

154. A method for making a semiconductor device, as defined in claims 127-128, wherein abutting the deep-level region with a material selected to enhance carrier transport comprises abutting a portion of the deep-level region with a semiconductor material different from that of the deep-level region.

155. A method for making a semiconductor device, as defined in claims 127-128, wherein abutting the deep-level region with a material selected to enhance carrier transport comprises abutting the deep-level region with a material having a Fermi-level or quasi-Fermi-level (under equilibrium or nonequilibrium conditions) which lies within the bandgap of the deep-level region.

156. A method for making a semiconductor device, as defined in claims 127-128, wherein abutting the deep-level region with a material selected to enhance carrier transport comprises abutting the deep-level region with a material having a Fermi-level or quasi-Fermi-level (under equilibrium or nonequilibrium

conditions) which lies between $0.2E_G$ and $0.8E_G$ above the valence-band in the bandgap of the deep-level region.

157. A method for making a semiconductor device, as defined in claims 127-128, wherein abutting the deep-level region with a material selected to enhance carrier transport comprises abutting the deep-level region with a material having a Fermi-level or quasi-Fermi-level (under equilibrium or nonequilibrium conditions) which lies between $0.3E_G$ and $0.7E_G$ above the valence-band in the bandgap of the deep-level region.

158. A method for making a semiconductor device, as defined in claims 127-128, wherein abutting the deep-level region with a material selected to enhance carrier transport comprises abutting the deep-level region with a material having a Fermi-level or quasi-Fermi-level (under equilibrium or nonequilibrium conditions) which lies between $0.4E_G$ and $0.6E_G$ above the valence-band in the bandgap of the deep-level region.

159. A method for making a semiconductor device, as defined in claims 127-128, wherein abutting the deep-level region with a material selected to enhance carrier transport comprises abutting the deep-level region with a material having a Fermi-level or quasi-Fermi-level (under equilibrium or nonequilibrium

conditions) which lies closer to the upper state than to the lower state of the desired transition(s) in the deep-level region.

160. A method for making a semiconductor device, as defined in claims 127-128, wherein abutting the deep-level region with a material selected to enhance carrier transport comprises abutting the deep-level region with a material having a Fermi-level or quasi-Fermi-level (under equilibrium or nonequilibrium conditions) which lies closer to the lower state than to the upper state of the desired transition(s) in the deep-level region.

161. A semiconductor device comprising:

a first region of semiconductor material having relatively few deep-level states; and,

a second region of semiconductor material having many deep-level states which form a pseudo-energy band which is closer to the valence-band than to the conduction-band in the second region.

162. A semiconductor device comprising:

a first region of semiconductor material having relatively few deep-level states; and,

a second region of semiconductor material having many deep-level states which form a pseudo-energy band which is

closer to the conduction-band than to the valence-band in the second region.

163. Material and method for making a semiconductor device wherein the deep-level concentration in different layers can be changed by changing the growth temperature.

164. Material and method for making a semiconductor device wherein the deep-level concentration in different layers can be changed by lowering the growth temperature.

165. Material and method for making a semiconductor device wherein the deep-level concentration in different layers can be changed by changing the growth rate.

166. Material and method for making a semiconductor device wherein the deep-level concentration in different layers can be changed by lowering the growth rate.

167. Material and method for making a semiconductor device wherein the deep-level concentration in different layers can be changed by a combination of changing the growth rate at different growth temperatures.

168. Material and method for making a semiconductor device wherein the deep-level concentration in different layers can be changed by a combination of lowered growth rate at lowered growth temperatures.

169. Material and method for making a semiconductor device wherein one or more of its electrical contacts are located directly on the top surface of the sample.

170. Material and method for making a semiconductor device wherein two or more of its electrical contacts are located directly on the top surface of the sample.

171. Material and method for making a semiconductor device, containing a deep-level region, wherein one or more of its electrical contacts has a nonlinear current-voltage characteristic.

172. Material and method for making a semiconductor device, containing a deep-level region, wherein one or more of its electrical contacts has a sharply increasing and nonlinear current-voltage characteristic.

173. Material and method for making a semiconductor device, containing a deep-level region, wherein one or more of its electrical contacts is ohmic.

174. Material and method for making a semiconductor device, containing a deep-level region, wherein one or more of its electrical contacts exhibits a diode-like current-voltage characteristic.

175. Material and method for making a semiconductor device, containing a deep-level region, where the device can be operated

with the voltage at the top contact (on the surface of the wafer) positive with respect to the voltage at the substrate.

176. Material and method for making a semiconductor device, containing a deep-level region, where the device can be operated with the voltage at the top contact (on the surface of the wafer) negative with respect to the voltage at the substrate.

177. Material and method for making a semiconductor device, containing a deep-level region, where the device can be operated with the voltage at the top contact (on the surface of the wafer) either positive or negative with respect to the voltage at the substrate.

178. Material and method for making a semiconductor deep-level device, where the sign of the operating voltage can be used to change the optical properties of the semiconductor deep-level device.

179. Material and method for making a semiconductor deep-level device, where the sign of the operating voltage can be used to change the selection-rules of the deep-level optical transitions in the semiconductor deep-level device.

180. Material and method for making a semiconductor deep-level device, where the sign of the operating voltage can be used to change the strength of the deep-level optical transitions in the semiconductor deep-level device.

181. Material and method for making a semiconductor deep-level device, where the sign of the operating voltage can be used to change the spectral shape of the deep-level optical transitions in the semiconductor deep-level device.

182. Material and method for making a semiconductor deep-level device, where the magnitude of the operating voltage can be used to change the optical properties of the semiconductor deep-level device.

183. Material and method for making a semiconductor deep-level device, where the magnitude of the operating voltage can be used to change the selection-rules of the deep-level optical transitions in the semiconductor deep-level device.

184. Material and method for making a semiconductor deep-level device, where the magnitude of the operating voltage can be used to change the strength of the deep-level optical transitions in the semiconductor deep-level device.

185. Material and method for making a semiconductor deep-level device, where the magnitude of the operating voltage can be used to change the spectral shape of the deep-level optical transitions in the semiconductor deep-level device.

186. Method for making a material and a semiconductor device having a deep-level which is above the middle of the bandgap.

187. Method for making a material and a semiconductor device having a local maximum in the deep-level density-of-states which is above the middle of the bandgap.

188. Method for making a material and a semiconductor device having deep-level states, whose density-of-states are within a factor of 4 of a local maximum in the density-of-states, lie above the middle of the bandgap.

189. Claim 186, where the device utilizes the conduction-band-to-deep-level transition (in order to reduce the number of possible DDCH Auger processes).

190. Claim 186, where the device utilizes the valence-band-to-deep-level transition (in order to easily fill the deep-level from the conduction-band).

191. Claim 187, where the device utilizes the conduction-band-to-deep-level transition (in order to reduce the number of possible DDCH Auger processes).

192. Claim 187, where the device utilizes the valence-band-to-deep-level transition (in order to easily fill the deep-level from the conduction-band).

193. Claim 188, where the device utilizes the conduction-band-to-deep-level transition (in order to reduce the number of possible DDCH Auger processes).

194. Claim 188, where the device utilizes the valence-band-to-deep-level transition (in order to easily fill the deep-level from the conduction-band).

195. Method for making a material and a semiconductor device having a deep-level which is below the middle of the bandgap.

196. Method for making a material and a semiconductor device having a local maximum in the deep-level density-of-states which is below the middle of the bandgap.

197. Method for making a material and a semiconductor device havingdeep-level states, whose density-of-states are within a factor of 4 of a local maximum in the density-of-states, lie below the middle of the bandgap.

198. Claim 195, where the device utilizes the valence-band-to-deep-level transition (in order to reduce the number of possible DDCH Auger processes).

199. Claim 195, where the device utilizes the conduction-band-to-deep-level transition (in order to easily fill the deep-level from the valence-band).

200. Claim 196, where the device utilizes the valence-band-to-deep-level transition (in order to reduce the number of possible DDCH Auger processes).

201. Claim 196, where the device utilizes the conduction-band-to-deep-level transition (in order to easily fill the deep-level from the valence-band).

202. Claim 197, where the device utilizes the valence-band-to-deep-level transition (in order to reduce the number of possible DDCH Auger processes).

203. Claim 197, where the device utilizes the conduction-band-to-deep-level transition (in order to easily fill the deep-level from the valence-band).

204. Method for making material and semiconductor device for which the deep-level density-of-states (averaged over energy) between the dominant-deep-level energy-band and the conduction-band is higher than the deep-level density-of-states (averaged over energy) between the dominant-deep-level energy-band and the valence-band. (See Figure 11.)

205. Claim 204, where the device utilizes the valence-band-to-deep-level-energy-band transition (sensible when carriers are able to de-excite quickly (faster than the valence-band-to-deep-level-energy-band optical transition time) from the conduction-band to the deep-level energy-band).

206. Claim 204, where the device utilizes the conduction-band-to-deep-level-energy-band transition (sensible when carriers are not able to de-excite quickly (as compared with the valence-band-to-deep-level-energy-band optical transition time) from the conduction-band to the deep-level energy-band).

207. Method for making material and semiconductor device for which the total number of deep-levels (density-of-states

integrated over energy) between the dominant-deep-level energy-band (peak in the deep-level density-of-states) and the conduction-band is higher than the total number of deep-levels (density-of-states integrated over energy) between the dominant-deep-level energy-band (peak in the deep-level density-of-states) and the valence-band. (See Figure 11.)

208. Claim 207, where the device utilizes the valence-band-to-deep-level-energy-band transition (sensible when carriers are able to de-excite quickly (faster than the valence-band-to-deep-level-energy-band optical transition time) from the conduction-band to the deep-level energy-band).

209. Claim 207, where the device utilizes the conduction-band-to-deep-level-energy-band transition (sensible when carriers are not able to de-excite quickly (as compared with the valence-band-to-deep-level-energy-band optical transition time) from the conduction-band to the deep-level energy-band).

210. Method for making material and semiconductor device for which the deep-level density-of-states (averaged over energy) between the dominant-deep-level energy-band and the valence-band is higher than the deep-level density-of-states (averaged over energy) between the dominant-deep-level energy-band and the conduction-band. (See Figure 10.)

211. Claim 210, where the device utilizes the conduction-band-to-deep-level-energy-band transition (sensible when carriers are

able to de-excite quickly (faster than the conduction-band-to-deep-level-energy-band optical transition time) from the valence-band to the deep-level energy-band);

212. Claim 210, where the device utilizes the valence-band-to-deep-level-energy-band transition (sensible when carriers are not able to de-excite quickly (as compared with the conduction-band-to-deep-level-energy-band optical transition time) from the valence-band to the deep-level energy-band).

213. Method for making material and semiconductor device for which the total number of deep-levels (density-of-states integrated over energy) between the dominant-deep-level energy-band (peak in the deep-level density-of-states) and the valence-band is higher than the total number of deep-levels (density-of-states integrated over energy) between the dominant-deep-level energy-band (peak in the deep-level density-of-states) and the conduction-band. (See Figure 10.)

214. Claim 213, where the device utilizes the conduction-band-to-deep-level-energy-band transition (sensible when carriers are able to de-excite quickly (faster than the conduction-band-to-deep-level-energy-band optical transition time) from the valence-band to the deep-level energy-band);

215. Claim 213, where the device utilizes the valence-band-to-deep-level-energy-band transition (sensible when carriers are not able to de-excite quickly (as compared with the conduction-

band-to-deep-level-energy-band optical transition time) from the valence-band to the deep-level energy-band).

216. Method for making material and semiconductor device where the average concentration of deep-centers is greater than $0.001\alpha^3/8$, where $1/\alpha$ is the radius of the spatial extent of the deep-center bound-state.

217. Method for making material and semiconductor device where the average concentration of deep-centers is greater than $0.001\alpha^3/8$, where $1/\alpha$ is given by:

$$1/\alpha = |\langle s|z|z\rangle| \left[E_G / \left[E_d (E_G - E_d) \right] \right]^{1/2}$$

where E_d is the deep-level (as measured from the valence-band edge), and E_G is the bandgap energy, and $\langle s|z|z\rangle$ is the Kane matrix element.

218. Method for making material and semiconductor device having a conduction-band quasi-Fermi-level of between midgap and $300\hbar^2\alpha^2/2m_{eff}$ above the conduction-band edges, where m_{eff} is the conduction-band effective mass.

219. Method for making material and semiconductor device having a valence-band quasi-Fermi-level of between midgap and $300\hbar^2\alpha^2/2m_{eff}$ below the valence-band edges, where m_{eff} is the valence-band effective mass.

220. Method for making material and semiconductor device having a conduction-band quasi-Fermi-level above midgap.

221. Method for making material and semiconductor device having a valence-band quasi-Fermi-level of below midgap.

222. Method for making material and semiconductor device having a conduction-band quasi-Fermi-level of between midgap and $400\hbar^2\alpha^2/2m_{eff}$ above the conduction-band edges, where m_{eff} is the conduction-band effective mass.

223. Method for making material and semiconductor device having a valence-band quasi-Fermi-level of between midgap and $400\hbar^2\alpha^2/2m_{eff}$ below the valence-band edges, where m_{eff} is the valence-band effective mass.

224. Method for making material and semiconductor device which utilizes deep-level-to-conduction-band transitions involving a transition energy of $E_G - E_d + N\ \hbar^2\alpha^2/2m_{eff}$, where N a real number

between 0.0 and 300, and where m_{eff} is the conduction-band effective mass.

225. Method for making material and semiconductor device which utilizes deep-level-to-valence-band transitions involving a transition energy of $E_G - E_d + N\ \hbar^2\alpha^2/2m_{eff}$, where N a real number between 0.0 and 300, and where m_{eff} is the valence-band effective mass.

226. Method for making material and semiconductor device which utilizes deep-level-to-conduction-band optical transitions involving a photon energy of $E_G - E_d + N\ \hbar^2\alpha^2/2m_{eff}$, where N a real number between 0.0 and 300, and where m_{eff} is the conduction-band effective mass.

227. Method for making material and semiconductor device which utilizes deep-level-to-valence-band optical transitions involving a photon energy of $E_G - E_d + N\ \hbar^2\alpha^2/2m_{eff}$, where N a real number between 0.0 and 300, and where m_{eff} is the valence-band effective mass.

228. Method for making material and semiconductor device which operates at a current (an injection current or photocurrent or leakage current) whose magnitude is greater than (or equal to) N/τ, where τ is the bigger of the quantities: optical transition lifetime or nonradiative recombination lifetime; and N is the smaller of the quantities: the deep-center concentration or the hole or electron concentration corresponding to the quasi-Fermi-levels given in claims 220 and 221. By operating current, I include the short-circuit current which results from shorting out a device normally operated in open-circuit mode.

229. Method for making material and semiconductor device which operates at a current (an injection current or photocurrent or leakage current) whose magnitude is greater than (or equal to) N/τ, where τ is the bigger of the quantities: optical transition lifetime or nonradiative recombination lifetime; and N is the smaller of the quantities: the deep-center concentration or the hole or electron concentration corresponding to the quasi-Fermi-levels given in claims 222 and 223. By operating current, I include the short-circuit current which results from shorting out a device normally operated in open-circuit mode.